VLSI DESIGN (THEORY) EE-405

Pre-requisite: Electronic Circuit Design – I, Digital Logic Design
Credit Hours 03
Contact Hours 48

RECOMMENDED BOOKS

Modern VLSI System Design by Wayne Wolf

Reference Books

Neil Weste, David Harris "CMOS VLSI Design, A Circuit and System Perspective", 3rd Edition 2004, Addison Wesley

OBJECTIVE OF COURSE

VLSI Design and Design Tools, Fabrication of VLSI Devices: Concepts and Techniques used in the Fabrication of VLSI Integrated Circuits, Basic Semiconductor and MOSFET Theory, Integrated Circuit Fabrication, Integrated Circuit Layout, NMOS & CMOS Logic Design, Simulation of Circuit, Analog Circuit Design, Memory and Processor Design, Testing of VLSI System Architecture. VLSI Designing Using Hardware Description Languages: Programming in Verilog and VHDL, Netlisting, Simulation and Testing.

S.NO	CLO/PLOS MAPPING	DOMAIN	PLO
01	Be able to use mathematical methods and circuit analysis models in **analysis** of CMOS digital electronics circuits, including logic components and their interconnect	C3	01
02	Be able to **apply** CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic e□ects.	C3	02
03	**Description** of the characteristics of CMOS circuit construction and the comparison between di□erent state-of-the-art CMOS technologies and processes.	C2	02

COURSE CONTENTS

Fundamental Concepts of VLSI Design

- Introduction
- Conductors, insulators, semiconductors, intrinsic material, extrinsic material
- Integrating circuits manufacturing technology economics

- CMOS Technology
- Power consumption, design and testability

Integrated Circuit Design Techniques

- Design Abstraction
- Translation and layout fabrication steps
- Structure of a transistor
- Transistor modeling parasitic, tubties and latch up
- Leakage and sub threshold currents
- Wires and Vias , skin Effect

SCMOS based Design Rules

- Stick diagrams, physical layout, fabrication Errors
- Static complementary gates
- Switch logic
- Delay through Resistive interconnects
- Low power gates
- Delay through Inductive interconnect

Standard Cell Based Layout

- Fan-out path delay Cross Talk, Buffer insertion
- Latches and flip flop
- Clocking Disciplines
- Sequential system design
- Floor planning methods
- Design validation
- Off chip Connections