DIGITAL LOGIC DESIGN (THEORY) (EE210)

Pre-requisite: No
Credit Hours: 03
Contact Hours: 48

RECOMMENDED BOOK

- M. Morris Mano, Michael D. Ciletti, "Digital Design with an Introduction to the Verilog HDL", 5th Edition, 2013, Pearson. ISBN: 978-0-13-277420-8

REFERENCE BOOK(S)

- Thomas L. Floyd, "Digital Fundamentals",11th Edition,2015, Pearson ISBN: 978-0-13-273796-8

OBJECTIVE OF COURSE

One of the main objectives of this course is to acquaint students with fundamental concepts of digital logic design. To explain the basic Boolean algebra laws, theorems and gate level minimization techniques. To demonstrate the basic designing techniques of combinational and synchronous logic. To give the basic ideas how to design and analyze the logic circuit.

S. NO	CLO/PLOS MAPPING	DOMAIN	PLO
01	To understand and apply the basic Boolean algebra theorems and gate level minimization techniques to analyze logic circuits		**01**
02	Identify, formulate and solve problems related to digital logic design		**02**
03	To design and analyze some basic combinational logic circuits		**03**
04	To utilize state machines technique / method to design and analyze some basic sequential logic circuits		**03**

RECOMMENDED BOOK

- DLD Lab Manual

REFERENCE BOOK(S)

- Thomas L. Floyd, "Digital Fundamentals",11th Edition,2015, Pearson ISBN: 978-0-13-273796-8
- Morris Mano, Charles R. Kime, Tom Martin, "Logic and Computer Design Fundamentals", 5th Edition, 2015, Pearson. ISBN: 978-0-13-376063-7

COURSE CONTENTS

Review of Number systems

- Binary, Octal, Hexadecimal, Base-N number system, R's Complement, (R-1)'s Complement
- Signed, unsigned integers and their arithmetic functions
- BCD Codes, BCD Addition
- 2421 Codes, Excess-3 Codes, 8 4-2-1 Codes, ASCII Codes, Gray Codes

Boolean Algebra

- Theorems and Properties of Boolean algebra. Boolean Functions
- Boolean Functions ,Simplification of Boolean Functions using Boolean Theorems
- Canonical Form (Sum of Min terms, Product of Max terms)
- Standard Form (Sum of Products, Product of Sums)
- Digital Logic Gates
- Digital Logic Families

Gate Level minimization

- Gate Level minimization using up to 6 variable k-maps
- SOP Simplification
- POS Simplification
- Don't Care Conditions
- Logic implementation using NAND gates only
- Logic implementation using only NOR gates
- XOR Function
- Even & Odd Function

Parity Generation and Checking

Designing Combinational Logic

- BCD to Excess-3 Converter
- BCD to Gray Code Converter
- Adders: Half Adder, Full Adder, Ripple Carry Adder, Carry Look Ahead Adder,
- Subtractor over Flow, BCD Adder
- Binary Multiplier using Adders

- Magnitude Comparator
- Decoder, Implementation of Full Adder using Decoder
- Encoder, Priority Encoder
- Multiplexer, Boolean Function Implementation using MUX
- Three-State Gates, Designing MUX using Three-State Gate

Synchronous Sequential Logic.

- SR Latch, D Latch & Timing Diagrams
- SR Flip-Flop, D Flip-Flop, JK Flip-Flop, T Flip-Flop
- Edge Triggered and Level Triggered
- State Machines State Diagram, State Table
- Synchronous Sequential Circuit Designing using State Machines
- Moore and Mealy Machines, State Reduction Technique
- Registers, Asynchronous Counter, 4x4 SRAM