ADVANCED ELECTRONICS LABORATORIES

WORKSHOP ON CHIP PROCESS DESIGN & ANALYTICAL TESTING

In continuation to the previous workshops, Advanced Electronics Laboratories offer a 6-days workshop on ***CHIP PROCESS DESIGN AND ANALYTICAL TESTING*** for all of its graduate students who are entering into research phase from FALL 2016. The lab engineers and faculty members from Faculty of Engineering & Technology, Faculty of Basic and Applied Sciences and Iqra College are also encouraged to attend the workshop to gain the knowledge of technological processes of IC design as well as post-process reliability, efficiency and failure analysis of devices and nano-systems. The training will be conducted on internationally licensed softwares and R&D grade sophisticated machines in the laboratories.

Day 1 & Day 2: Introduction to State of the art Licenced tools	• Why Device Design is phenomenally important? • CMOS Scaling & Efficiency, IC Fabspecific design and processes • Road to technology files, ATHENA, ATLAS, BLAZE, LUMINOUS, ORGAN
Day 3 & Day 4: Advanced Electrical/Electro-Optical Characterizations	• Nano chip reliabality grade Hall Effect Chip level Characterizations • Multi-head Probe station assembeled with varaity of different device/circuit level techniques • Introduction to van der paw, Hall and Clover leaf patterens for Hall Analysis • Effect of Magnitization, Electric Field, Transient of bais sweeps, Resistivity/Conductivity Scans, Charge Carrier Cocentrations, Electon/Hole Mobilities for Chip level assesment • Practical hands on Open Circuit Voltage (Voc) and Short Circuit Current (Isc) for PV devices • Effect of Current Voltage (I-V) and Capcitance Voltage (C-V) profiling for research prospects • Introduction to very sophisticated characterization techniques; Charge Deep Level Transient Spectropcopy (Q-DLTS) and Photo stimulated Internal Field Transient Spectroscopy • Issues in device reliability
Day 5: Optical Assessment & Rapid Thermal Processing	• Optical profilometry and scanning of optical parameters like refractive index, dielectrics, extinction coefficients, thickness at subnano scales • Optical Characterization of *Si* based Quadrant photo detector (basic overview) • Hands on with multiple devices and samples, working out the electro-optics • Experimentation on Rapid thermal annealing machine, Technique of RT-CVD, RTO and RTP, ITRS specific Thermal budget
Day 6: Back End Processes	• Device's Metalization, Cleaning, Etching, Spin Coating, Baking. • Wet chemistry, contact development, Physical Layer Depostion, packaging etc.

AELP HIGHLIGHTS

- State of the art Device Design and Process Characterization Facilities under one roof
- Over 85 running scientific projects besides over 300 of Quality Assurance runs
- Problem converging on the forefronts of Micro & Nano Electronics, Photonics & Optoelectronics, Photovoltaic Engineering & Energy and Sensing & Detection
- 34% of the total running projects are from outside the IIUI including other universities, industry and national scientific organizations

Days: 24th to 29th Oct., 2016
Time: 10:00 AM – 4:00 PM
Venue:
Advanced Electronics Laboratories, Ibn-Khaldun Block, IIUI

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