Curriculum Vitae

Muhammad Haris Anis

EXPERIENCE

October 2011 – Present

International Islamic University www.iiu.edu.pk
Assistant Professor (Faculty of Engineering & Technology)

Courses Taught

- FPGA Based Design
- Fundamentals of Programming
- Object Oriented Programming
- System Programming
- Digital Logic Design
- ASIC Design
- Embedded System Design
- FPGA Based Design Lab
- Embedded System Design Lab

February 2011 – December 2011

National University of Science & Technology www.nust.edu.pk
Visiting Faculty (School of Electrical Engineering & Computer Sciences www.seecs.edu.pk)

Courses Taught

- Microprocessor Systems

June 2003- September 2011

Design, Development & verification experience, in the field of Embedded System Design and Digital Design for FPGAs and ASICs with different national & multinational companies.

EDUCATION

Master of Science in Computer Engineering.
University of Engineering and Technology, Taxila, Pakistan

Bachelor of Science in Computer Systems
National University of Science and Technology, Rawalpindi, Pakistan

Publications

- Athar Waseem, Aqdas Naveed, Sardar Ali, Muhammad Arshad, **Haris Anis,** Ijaz Mansoor Qureshi

"Compressive Sensing based Channel Estimation for Massive MIMO Communication Systems," Wireless

Communications and Mobile Computing, Article ID 6374764, Volume 2019, DOI: 10.1155/2019/6374764

(Impact Factor 1.6)

- Muhammad Bilal, **Haris Anis**, Najeeb Khan, Ijaz Qureshi, Jawad

Shah, Kushsairy A. Kadir

“**Reduction of Motion Artifacts in the Recovery of Undersampled DCE MR Images Using Data Binning and L+S Decomposition”**

Biomed Res Int. 2019 Apr 17;2019:6139785. doi: 10.1155/2019/6139785.

- Ashfaq, O. Mairaj, J. Raza, A. **Anis, H**.

Field Upgradeable Dynamically Reconfigurable Accelerated Firewall for Networks
Paper appeared in: SCONEST 2004, IEEE
Issue Date: 30-31 Dec. 2004, **On page(s):** 144 – 151, **Print ISBN:** 0-7803-8871-2
Digital Object Identifier: 10.1109/SCONES.2004.1564786, 03 January 2006